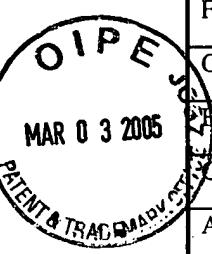


Tfu

First Named Inventor	Kirk D. Prall
Serial No.	10/786,765
Filing Date	February 25, 2004
Group Art Unit	2818
Examiner Name	Unknown
Confirmation No.	2857
Attorney Docket No.	400.266US01
Title: MULTI-LAYER MEMORY ARRAYS	

**GENERAL  
TRANSMITTAL  
FORM UNDER 37 CFR 1.8  
(LARGE ENTITY)**



Mail Stop: AMENDMENT  
Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

**Enclosures**

**The following documents are enclosed:**

- Supplemental Information Disclosure Statement (1 pg.); Form 1449 (1 pg.); 3 copies of cited references; U.S. reference(s) not included pursuant to 37 C.F.R. 1.98 (c)(2)(i);  
 An itemized return-receipt postcard

Leffert Jay & Polglaze, P.A.  
P.O. Box 581009  
Minneapolis, MN 55458-1009  
T - 612/312-2200  
F - 612/312-2250

**Please charge any additional fees or credit any overpayments  
to Deposit Account No. 501373.**

**CUSTOMER NO. 27073**

**Submitted By**

Name	Tod A. Myrum	Reg. No.	42,922	Telephone	(612) 312-2208
Signature	<i>Tod A. Myrum</i>			Date	02-28-05

**Certificate of Mailing**

I certify that this correspondence and the identified documents listed on this transmittal are being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop: AMENDMENT, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on February 28, 2005.

Name	Rhonda L. Foley	Signature	<i>Rhonda L. Foley</i>
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(LARGE ENTITY TRANSMITTAL UNDER 37 CFR § 1.8)

First Named Inventor	Kirk D. Prall
Serial No.	10/786,765
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**SUPPLEMENTAL  
INFORMATION  
DISCLOSURE  
STATEMENT**

Mail Stop: AMENDMENT  
 Commissioner for Patents  
 P.O. Box 1450  
 Alexandria, VA 22313-1450

In compliance with 37 C.F.R. §§ 1.56 and 1.97, *et seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified Application.

Pursuant to 37 C.F.R. 1.98 (a)(2)(i), as this application was filed after June 30, 2003, Applicant has not included copies of U.S. Patents or U.S. Patent Applications. Applicant respectfully requests that this Supplemental Information Disclosure Statement be entered and the references listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to MPEP §609, Applicant further requests that the Examiner initial next to each reference on the Form 1449 to indicate that the listed references have been considered. Applicant further requests that a copy of the initialed Form 1449 be returned with the next official communication.

As an Office Action has not yet issued in this application, Applicant believes that no fees are due. However, the Commissioner for Patents is hereby authorized to charge any additional fees to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2208.

Respectfully submitted,

Date: 02-28-05

  
 Tod A. Myrum  
 Reg. No. 42,922

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First Named Inventor	Kirk D. Prall	<b>INFORMATION DISCLOSURE STATEMENT FORM PTO-1449</b>
Serial No.	10/786,765	
Filing Date	February 25, 2004	
Group Art Unit	2818	
Examiner Name	Unknown	
Confirmation No.	2857	
Attorney Docket No.	400.266US01	
Title: MULTI-LAYER MEMORY ARRAYS		

Sheet 1 of 1

<b>U.S. Patent References</b>				
Examiner Initials	Document No.	Issue/Publication Date	Name	Filing Date
	6,034,882	03/07/2000	Johnson	11/16/1998
	6,735,104 B2	05/11/2004	Scheuerlein	05/16/2003
	6,822,903 B2	11/23/2004	Scheuerlein	03/31/2003

<b>Foreign Patent References</b>				
Examiner Initials	Foreign Patent	Name	Publication Date	Translation
	Country	No.		

<b>Other References</b>	
Examiner Initials	Author, Title, Date, Pages, etc.
	S. Herner et al., "Vertical p-I-n Polysilicon Diode With Antifuse for Stackable Field-Programmable ROM," IEEE Electron Device Letters, Vol. 25, No. 5, May 2004, pp. 271-273
	M. Johnson et al., "512-Mb PROM With a Three-Dimensional Array of Diode/Antifuse Memory Cells," IEEE Journal of Solid State Circuits, Vol. 38, No. 11, Nov. 2003, pp. 1920-1928
	F. Li et al., "Evaluation of SiO <sub>2</sub> Antifuse in a 3D-OTP Memory," IEEE Transactions on Device and Materials Reliability, Vol. 4, No. 3, Sept. 2004, pp. 416-421

Examiner Signature		Date Considered	
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\*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Based on Form PTO-FB-A820 Patent and Trademark Office, U.S. Department of Commerce